(RAM) 64. The ICH 70 controls operations between processor 60 and input/output (I/O) devices, for examples, a keyboard (KBD) 73 and a mouse 74. The ICH 70 also controls operations between processor 60 and peripheral devices, for examples, a drive 71 and a modem 72. In another embodiment, the MCH 65 and the ICH 70 may be integrated into a single component.

Please replace the paragraph beginning at page 8, line 7 and ending at page 8, line 22 with the following:

Figure 3 illustrates one embodiment of an interface. In one embodiment, the memory device 350 is configured with a standard flash interface 352 for testing device functionality at wafersort. The standard flash interface 352 includes 20 address pads 301-308, and 313-324; control pads 309, 311-312, and 336-338; configuration pad 339; supply pads 310, and 329-331; data (DQ) pads 325-328, and 332-335; and no connect (NC) pad 340. The control pads 309, 311-312, and 336-338 are used for control operations of the memory device 350, for examples, chip enable, output enable, reset, and status. Configuration pad 339 is used to select between the test interface and the other interfaces used, for example, during the programming and operation modes of memory device 350. During wafersort testing at the component manufacturer, data is loaded into and read from the memory device 350 on data pads 325-328 to test for defects. The 20 pad address configuration allows for accessing the memory device 350 in one cycle because the address information can be loaded in parallel, thereby allowing data to be read on the same cycle.

Please replace the paragraph beginning at page 9, line 6 and ending at page 9, line 17 with the following:

Figure 4 illustrates one embodiment of another interface. In one embodiment, interface 454 is a programming interface that may be used in programming the memory device with firmware. As previously discussed, programming is performed after the memory device 350 is assembled into a package and ready for assembly onto the motherboard 61 of Figure 1. During this time, memory device 450 is programmed with low level code to enable the startup of computer system 75 of Figure 1. Configuration pad 402 is bonded out in the packaged memory device 450 for selecting between the programming interface 454 and another interface, for example, a test interface 352 of Figure 3. In one embodiment, configuration pad 439 (used to select the test interface while in test mode) is not connected in the packaged memory device 450 as the test interface is no longer required.

A4

Please replace the paragraph beginning at page 9, line 18 and ending at page 10, line 2 with the following:

Access to the memory device 450 when assembled in a package may be accomplished through the programming interface 454. In one embodiment, the programming interface 454 is no longer used after the computer system 75 of Figure 1 is manufactured. In another embodiment, the programming interface may be used at a later time to reprogram the memory device 450 to operate with new technologies. Use of a programming interface 454 having a standard protocol may allow motherboard manufacturers to program the memory device 450 without requiring memory manufacturers to disclose a proprietary interface to motherboard manufacturers.

A5

Please replace the paragraph beginning at page 10, line 3 and ending at page 10, line 13 with the following:

In one embodiment, the programming interface 454 is an Address/Address multiplexer (A/A mux) interface having 11 address pads, 407 and 415-424; control pads 409, 411, 412, and 436-438; configuration pads 402 and 439; supply pads 410 and 429-431; data pads (DQ) 425-428 and 432-435; and no connect (NC) pads 401, 403-406, 408, 413-414, and 440. Data pads 425-428 are used to transfer firmware code data into memory locations (not shown) of memory device 450. The firmware code is programmed into particular memory locations of memory device 450 using address pads 407 and 415-424. Memory data addressing and storage is well known in the art. Accordingly, a detailed description of the memory device's internal components and operation is not provided herein.

Please replace the paragraph beginning at page 11, line 3 and ending at page 11, line 12 with the following:

Although a second cycle is required to load the memory device with a full address, the A/A Mux interface 454 is suited for use in programming operations where the additional time of using two cycles may not significantly contribute to the total cycle time of programming operations. The memory device 450 features that are dropped off due to use of a smaller pin count package may include, for example, locking. Locking is a protection feature that prevents the memory device from being intentionally or inadvertently overwritten. Because the A/A mux interface 454 is usually used only for programming, the additional circuit logic for locking may not be required.

Please replace the paragraph beginning at page 11, line 13 and ending at page 11, line 23 with the following:

Figure 5 illustrates yet another embodiment of an interface. In one embodiment, a third interface 556 is an operation interface. Operation interface 556 is used during operation of memory device 550 in computer system 75 on motherboard 61 of Figure 1. Operation interface 556 includes multiplexed address/data (A/DQ) pads 525-528; configuration pads 502 and 539; supply pads 510 and 529-531; control pads 511-512, 519-520, and 537-538; identification (ID) pads 521-524; clock (CLK) pad 509; and no connect pads 501, 503-508, 513-518, 532-536, and 540. A/DQ pads 525-528 may be multiplexed to function as both address and data pads. CLK pad 509 may be used to synchronize timing operations of memory device 550 with other chipset components on motherboard 61 of Figure 1.

Please replace the paragraph beginning at page 11, line 24 and ending at page 12, line 8 with the following:

Configuration pad 539 is used to select between the operation interface 556 and the programming interface 454 of Figure 4. The configuration pad 539 is coupled to interface selection circuitry that functions to switch between different memory device circuitry that is coupled to a particular I/O pad. For example, a particular I/O pad connected to control circuitry during operation of the memory device may be switched to address circuitry when programming the device. As such, additional dedicated I/O pads are not needed for programming operations. This eliminates the need for a larger pin count package required when a memory device contains dedicated pads for programming operations.

Please replace the paragraph beginning at page 12, line 14 and ending at page ~~19~~, line 7 with the following: